CLAIM LISTING

1. (Original) An apparatus that uses pseudo-differential voltage signaling, comprising:

a reference receiver that receives an undistributed reference voltage and in response produces a buffered voltage that is derived at least in part from the undistributed reference voltage;

signal receivers associated respectively with a plurality of signal voltages;

wherein an individual signal receiver receives both its associated signal voltage and the buffered voltage, and;

wherein said individual signal receiver evaluates its associated signal voltage and the buffered voltage to produce an output voltage.

2. (Original) An apparatus as recited in claim 1, wherein said individual signal receiver evaluates by comparing the associated signal voltage and the buffered voltage to produce an output voltage.

3. (Original) An apparatus as recited in claim 1, wherein the buffered voltage is the difference between the undistributed reference voltage and a distributed reference voltage.

4. (Original) An apparatus as recited in claim 1, wherein the buffered voltage is proportional to the undistributed reference voltage.

5. (Original) An apparatus as recited in claim 1, wherein the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage.

6. (Original) An apparatus as recited in claim 1, wherein the reference receiver also receives a distributed reference voltage that is received by the signal receivers, wherein the reference receiver is responsive to the distributed reference voltage and the undistributed reference voltage to produce the buffered voltage.

7. (Original) An apparatus as recited in claim 1, wherein the reference receiver also receives a distributed reference voltage that is received by the signal receivers, wherein the reference receiver compares the distributed reference voltage and the undistributed reference voltage to produce the buffered voltage.

8. (Original) An apparatus as recited in claim 1, wherein the reference receiver also receives a distributed reference voltage that is received by the signal receivers, wherein the reference receiver compares the distributed reference voltage and the undistributed reference voltage to produce the buffered voltage, the buffered voltage representing the difference between the distributed reference voltage and the undistributed reference voltage.

9. (Original) An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference receiver having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

10. (Original) An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference receiver having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance; and

wherein the reference receiver and the signal buffers are source-followers.

11. (Original) An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages.

12. (Original) An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages;

wherein the reference receiver and the signal buffers are source-followers.

13. (Original) An apparatus as recited in claim 1, wherein the reference receiver has a unity gain.

14. (Original) An apparatus as recited in claim 1, wherein:

the signal voltage has associated input capacitance and inductance that result in a resonant input frequency;

the reference receiver has a bandwidth that is significantly greater than the resonant input frequency.

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15. (Original) An apparatus as recited in claim 1, wherein:

the signal voltage has associated input capacitance and inductance that result in a resonant input frequency;

the reference receiver has a bandwidth of at least ten times the resonant input frequency.

16. (Original) An apparatus as recited in claim 1, wherein each signal voltage represents one of two values and the signal receivers compare the buffered voltage and the signal voltages to determine which of the two values is represented by each signal voltage.

17. (Original) An apparatus as recited in claim 1, the reference voltage and the buffered voltage being subject to similar impedances.

18. (Currently Amended) An apparatus as recited in claim 1, the reference voltages and signal voltage being subject to similar impedances, wherein coupled signal noise is introduced approximately equally in the buffered voltage and the plurality of pseudo-differential signal voltages, said approximately equal coupled signal noise being canceled in the evaluation performed by the signal receiver.

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19. (Original) An integrated circuit comprising:

a reference input that receives a common reference voltage;

a plurality of signal inputs configured to receive pseudo-differential signal voltages that represent values in terms of relationships between the pseudo-differential signal voltages and the common reference voltage;

a reference buffer that receives the common reference voltage and in response produces a buffered reference voltage;

signal comparators associated respectively with the plurality of pseudo-differential signal voltages, each signal comparator comparing the buffered reference voltage and one of the pseudo-differential signal voltages to determine the value represented by said one of the pseudo-differential signal voltages;

wherein the reference and signal inputs have similar impedances, coupled signal noise being introduced approximately equally in the buffered reference voltage and the plurality of pseudo-differential signal voltages, said approximately

equal coupled signal noise being canceled in the comparison performed by the signal comparators.

20. (Original) An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered reference voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

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21. (Original) An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered reference voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance; and

wherein the reference buffer and the signal buffers are source-followers.

22. (Original) An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages for comparison by the signal comparators.

23. (Original) An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages;

wherein the reference buffer and the signal buffers are source-followers.

24. (Original) An integrated circuit as recited in claim 19, wherein the reference buffer has a unity gain.

25. (Original) An integrated circuit as recited in claim 19, wherein:

the signal inputs have associated input capacitances and inductances that result in a resonant input frequency;

the reference buffer has a bandwidth that is significantly greater than the resonant input frequency.

26. (Original) An integrated circuit as recited in claim 19, wherein:

the signal input has associated input capacitance and inductance that result in a resonant input frequency;

the reference buffer has a bandwidth of at least ten times the resonant input frequency.

27. (Original) An integrated circuit as recited in claim 19, wherein each signal voltage represents one of two values and the signal comparators compare the buffered reference voltage and the signal voltages to determine which of the two values is represented by each signal voltage.

28. (Original) An integrated circuit as recited in claim 19, the reference and signal inputs having matching impedances.

29. (Original) A system comprising:

a first integrated circuit that transmits a common reference voltage and a plurality of pseudo-differential signal voltages, wherein the pseudo-differential signal voltages represent values in terms of relationships between the pseudo-differential signal voltages and the common reference voltage;

a second integrated circuit that receives the common reference voltage and the plurality of pseudo-differential signal voltages;

the second integrated circuit having a reference buffer that receives the common reference voltage and in response produces a buffered reference voltage;

the second integrated circuit having signal comparators associated respectively with the plurality of pseudo-differential signal voltages, each signal comparator comparing the buffered reference voltage and a respective one of the pseudo-differential signal voltages to determine the value represented by said one of the pseudo-differential signal voltages;

wherein the second integrated circuit is configured to introduce approximately equal coupled signal noise in the buffered reference voltage and the plurality of pseudo-differential signal voltages, said approximately equal coupled signal noise being canceled in the comparisons performed by the signal comparators.

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30. (Original) A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject in the second integrated circuit to a signal capacitance;

the buffered reference voltage being subject in the second integrated circuit to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

31. (Original) A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject in the second integrated circuit to a signal capacitance;

the buffered reference voltage being subject in the second integrated circuit to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance; and

wherein the reference buffer and the signal buffers are source-followers.

32. (Original) A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages.

33. (Original) A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages;

wherein the reference buffer and the signal buffers are source-followers.

34. (Original) A system as recited in claim 29, wherein the reference buffer is a unity gain amplifier.

35. (Original) A system as recited in claim 29, wherein:

the second integrated circuit has signal inputs that receive the plurality of signal voltages, the signal inputs having associated input capacitance and inductance that result in a resonant input frequency;

the reference buffer has a bandwidth that is significantly greater than the resonant input frequency.

36. (Original) A system as recited in claim 29, wherein:

the second integrated circuit has signal inputs that receive the plurality of signal voltages, the signal inputs having associated input capacitance and inductance that result in a resonant input frequency;

the reference buffer has a bandwidth of at least ten times the resonant input frequency.

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37. (Original) A system as recited in claim 29, wherein each pseudo-differential signal voltage represents one of two values and the comparators compare the buffered reference voltage and the pseudo-differential signal voltages to determine which of the two values is represented by each pseudo-differential signal voltage.

38. (Original) A system as recited in claim 29, wherein the second integrated circuit has signal inputs that receive the pseudo-differential signal voltages and a reference input that receives the common reference voltage, the reference and signal inputs having similar impedances.

39. (Original) A method comprising:

receiving a reference voltage;

receiving a plurality of signal voltages;

producing a buffered voltage based at least in part on the reference voltage;

evaluating the buffered voltage and one of the signal voltages to determine a value represented by said one of the signal voltages.

40. (Original) A method as recited in claim 39, wherein the evaluating comprises comparing said one of the signal voltages and the buffered voltage to produce an output voltage.

41. (Original) A method as recited in claim 39, wherein the buffered voltage is the difference between an undistributed reference voltage and a distributed reference voltage.

42. (Original) A method as recited in claim 39, wherein the buffered voltage is proportional to the reference voltage.

43. (Original) A method as recited in claim 39, wherein the buffered voltage represents the noise of the signal voltages.

44. (Original) A method as recited in claim 39, said producing comprising comparing a distributed reference voltage that is received by the signal receivers and an undistributed reference voltage that is not received by the signal receivers.

45. (Original) A method as recited in claim 39, said producing comprising comparing a distributed reference voltage that is received by the signal receivers and a undistributed reference voltage that is not received by the signal receivers, the buffered voltage representing the difference between the undistributed reference voltage and the distributed reference voltage.

46. (Original) A method as recited in claim 39, further comprising:

buffering the signal voltages with signal buffers to produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

said producing the buffered voltage being performed with a reference buffer, the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

47. (Original) A method as recited in claim 39, further comprising:

buffering the signal voltages with source-follower signal buffers to produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

said producing the buffered voltage being performed with a source-follower reference buffer, the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

48. (Original) A method as recited in claim 39, further comprising:

buffering the signal voltages to produce buffered signal voltages.

49. (Original) A method as recited in claim 39, further comprising:

buffering the signal voltages with source-followers to produce buffered signal voltages.

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50. (Original) A method as recited in claim 39, wherein:

the signal voltages are received by signal inputs having associated input capacitances and inductances that define a resonant frequency;

producing the buffered voltage with a unity gain buffer having a bandwidth that is significantly greater than the resonant frequency.

51. (Original) A method as recited in claim 39, wherein:

the signal voltages are received by signal inputs having associated input capacitances and inductances that define a resonant input frequency;

producing the buffered voltage with a unity gain buffer having a bandwidth of at least ten times the resonant input frequency.

52. (Original) A method as recited in claim 39, wherein:

the reference voltage is received by a reference input;

the signal voltages are received by signal inputs; and

the reference and signal inputs have similar impedances.

53. (Original) A method as recited in claim 39, further comprising introducing coupled signal noise approximately equally in the buffered reference voltage and the plurality of signal voltages, said approximately equal coupled signal noise being canceled in the comparing.

54. (Original) An apparatus that uses pseudo-differential voltage signaling, comprising:

signal receivers associated respectively with a plurality of signal voltages;

a reference receiver that receives both an undistributed reference voltage and a distributed reference voltage, wherein the distributed reference voltage is distributed to the signal receivers and the undistributed reference voltage is not distributed to the signal receivers;

wherein the reference receiver evaluates the undistributed reference voltage and the distributed reference voltage to produce a buffered voltage that represents the difference between the undistributed reference voltage and the distributed reference voltage;

wherein an individual signal receiver receives both its associated signal voltage and the buffered voltage; and

wherein said individual signal receiver adjusts its associated signal voltage by the buffered voltage to produce an output voltage.

55. (Original) An apparatus as recited in claim 54, wherein said signal receivers are two-stage receivers.

56. (Original) An apparatus as recited in claim 54, wherein said signal receivers are two-stage receivers, the second stage of the receivers adjusting the signal voltages.

57. (Original) An apparatus as recited in claim 54, wherein the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage.

58. (Original) An apparatus as recited in claim 54, wherein the buffered voltage is a differential voltage.

59. (Original) An integrated circuit that uses pseudo-differential voltage signaling, comprising:

two-stage receivers associated respectively with a plurality of signal voltages;

a reference receiver that receives both an undistributed reference voltage and a distributed reference voltage, wherein the distributed reference voltage is distributed to the signal receivers and the undistributed reference voltage is not distributed to the signal receivers;

wherein the reference receiver compares the undistributed reference voltage and the distributed reference voltage to produce a buffered voltage that represents

the difference between the undistributed reference voltage and the distributed reference voltage;

wherein the first stage of an individual signal receiver compares its associated signal voltage to the distributed reference voltage to produce a voltage differential signal; and

wherein the second stage of said individual two-stage receiver adjusts the voltage differential signal by the buffered voltage to produce an output voltage.

60. (Original) An apparatus as recited in claim 59, the two-stage receiver has an input impedance similar to that of the reference receiver.

61. (Original) An apparatus as recited in claim 59, wherein the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage.

62. (Original) An apparatus as recited in claim 59, wherein the buffered voltage is a differential voltage.

63. (Original) A system comprising:

a first integrated circuit that transmits a common reference voltage and a plurality of pseudo-differential signal voltages, wherein the pseudo-differential signal voltages represent values in terms of relationships between the pseudo-differential signal voltages and the common reference voltage;

a second integrated circuit that receives the common reference voltage and the plurality of pseudo-differential signal voltages;

the second integrated circuit having a reference receiver that receives the common reference voltage and in response produces a buffered voltage;

the second integrated circuit having two-stage signal receivers associated respectively with the plurality of pseudo-differential signal voltages, each two-stage signal receiver adjusting one of the pseudo-differential signal voltages by the buffered voltage to produce an output voltage.

64. (Original) A system as recited in claim 63, wherein each two-stage signal receiver has an input impedance similar to that of the reference receiver.

65. (Original) A system as recited in claim 63, wherein:

the reference receiver compares a distributed common reference voltage to an undistributed common reference voltage to produce the buffered voltage;

the first stage of an individual two-stage signal receiver compares its associated pseudo-differential signal voltage to a distributed reference voltage to produce a voltage differential signal; and

the second stage of said individual two-stage signal receiver adjusts the voltage differential signal by the buffered voltage to produce an output voltage.

66. (Original) A system as recited in claim 63, wherein the buffered voltage represents the noise of the signal voltages.

67. (Original) A system as recited in claim 63, wherein the buffered voltage is a differential voltage.